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EXAMINER	
MEONSKE, TONIA L	

ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 02/19/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/748,077	COFLER ET AL.	
	Examiner	Art Unit	
	Tonia L Meonske	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 April 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *22 December 2000* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *5 and 6*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. This application lacks formal drawings. The informal drawings filed in this application are acceptable for examination purposes. When the application is allowed, applicant will be required to submit new formal drawings.

Specification

2. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 17, 19, 22, and 24 are rejected under 35 U.S.C. 102(b) as being clearly anticipated by Alpert et al., US Patent 5,621,886.

5. Referring to claim 17, Alpert et al. have taught a computer system for executing instructions in a first, user mode and a second, debug mode (Alpert et al., abstract), the computer system comprising:

a. a first store for holding user instructions (Figure 3, elements 345-385);

b. a second store for holding debug instructions, wherein the debug instructions are held in the second store in association with debug attributes, wherein said debug attributes include a stall attribute (Figure 3, element 320);

c. a fetch unit for selectively fetching instructions from the first or second store depending on the mode of the computer system (Figure 3, There is inherently a fetch unit that fetches either the debug instructions or the next sequential instruction depending on whether the computer system is operating in a debug mode.);

d. a decode unit for decoding said instructions and reading said attributes (Column 5, lines 50-60, In order for the instruction attributes to be present they must have inherently been decoded.); and

e. an emulation unit which includes control circuitry which cooperates with the decode unit to selectively set the decode unit into a stall state by issuance of a stall signal (column 11, line 33-column 12, line 7) wherein the decode unit includes stall control circuitry which is responsive to reading of a stall attribute or receipt of a stall signal from the emulation unit to place the decode unit into a stall state (Figure 4, Figure 5, element 530, column 11, line 35-column 12, line 9).

6. Referring to claim 19, Alpert et al. have taught a computer system according to claim 17, as described above, and wherein the debug code comprises a plurality of divert routines allowing debug functions to be implemented by the computer system (Alpert et al., Figure 2, element 240, column 9, lines 5-20).

7. Referring to claim 22, Alpert et al. have taught a computer system according to claim 17, as described above, which includes at least one pipelined execution unit for executing said instructions (Column 7, lines 28-34, The Pentium execution units are pipelined.).

8. Referring to claim 24, Alpert et al. have taught a method of setting a stall state of a computer system which comprises a fetch unit for fetching instructions to be executed (Figure

3, There is inherently a fetch unit that fetches either the debug instructions or the next sequential instruction.) and a decode unit for decoding said instructions (Column 5, lines 50-60, In order for the instruction to be executed, a decode unit must have inherently decoded the instruction.), wherein the stall state is set selectively at the decode unit by reading stall attributes associated with debug instructions in a debug mode (Figure 4, Figure 5, element 530, column 11, line 35-column 12, line 9), or by receipt of a stall command responsive to certain conditions when executing user instructions in a user mode (This condition is not necessary to be present in the reference in order for the reference to read on the claim as the claim includes the "or" alternative claim language.).

Claim Rejections - 35 USC § 103

9. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

10. Claims 1, 3, 4, 5, 6, 7, 8, 9, 11, 12, 13, 14, 15, 16, 18, 20, 21, and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Karp et al., US Patent 5,748,936, in view of Alpert et al., US Patent 5,621,886.

11. Referring to claim 1, Karp et al. have taught a computer system for executing predicated instructions wherein each instruction includes a guard, the value of which determines whether or not that instruction is executed (Karp et al., column 5, line 62-column 6, line 3), the computer system comprising:

a. a fetch unit for fetching instructions to be executed; a decode unit for decoding said instructions (Karp et al., column 5, lines 23-27);

b. at least one pipelined execution unit for executing decoded instructions and being associated with a guard register file holding values of the guards to allow resolution of the guards to be made to determine whether an instruction is committed (Karp et al., Column 5, line 23-column 6, line 3).

12. Karp et al. have not specifically taught an emulation unit including control circuitry which cooperates with the decode unit to selectively control the decode unit to implement step-by-step execution of an instruction sequence.

13. Alpert et al have taught an emulation unit including control circuitry which cooperates with the decode unit to selectively control the decode unit to implement step-by-step execution of an instruction sequence (Alpert et al., column 11, line 33-column 12, line 8) for the purpose of providing the programmer with valuable tools for looking at the dynamic state of the processor after each instruction (Alpert et al., column 1, lines 27-36, column 1, line 65-column 2, line 4). It would have been obvious to one of ordinary skill in the art at the time the invention was made to have the invention of Karp et al., include the emulation unit, as taught by Alpert et al., for the desirable purpose of providing the programmer with valuable tools for looking at the dynamic state of the processor after each instruction (Alpert et al., column 1, lines 27-36, column 1, line 65-column 2, line 4).

14. Furthermore, Karp et al. have not taught that for each committed instruction, a divert routine is executed by the computer system and for each noncommitted instruction the next instruction in the instruction sequence is executed. However, Alpert et al. have taught for each

committed instruction, a divert routine is executed (Alpert et al., Figure 3, elements 2, 4, and 6, column 12, lines 59-65). Furthermore, Alpert et al. have taught disabling debug breakpoints when they are not of interest to the programmer in order to improve the system performance (Alpert et al., column 9, lines 40-column 10, line 6). Instructions that are not committed are not of interest to the programmer as non-committed instructions do not change the architectural state of the processor. Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to have the invention of Karp et al., include for each committed instruction, executing a divert routine, as taught by Alpert et al., (Alpbert et al., Figure 3, elements 2, 4, and 6, column 12, lines 59-65) and for each noncommitted instruction the next instruction in the instruction sequence is executed, for the desirable purpose of disabling unnecessary debug breakpoints in order to improve system performance (Alpert et al., column 9, lines 40-column 10, line 6).

15. Referring to claim 3, Karp et al. in combination with Alpert et al. have taught a computer system according to claim 1, as described above, and which includes a program memory for holding said. instructions to be executed (Karp et al., Figure 1, element 24, column 5, lines 23-25).

16. Referring to claim 4, Karp et al. in combination with Alpert et al. have taught a computer system according to claim 1, as described above, and wherein the emulation unit is associated with an emulation program memory which holds a plurality of divert routines (Alpert et al., Figure 2, element 240, column 9, lines 5-20).

17. Referring to claim 5, Karp et al. in combination with Alpert et al. have taught a computer system according to claim 1, as described above, and wherein, for each instruction in the sequence, the decode unit is operable to issue a request to the execution pipeline for guard resolution (Karp et al., column 5, line 57-column 7, line 32), the guard resolution being transmitted to the control circuitry of the emulation unit which implements said divert routine if the instruction is committed (Combination of Karp et al. with Alpert et al., In order to benefit from this combination, the guard resolution must be transmitted to the control circuitry of the emulation unit.).

18. Referring to claim 6, Karp et al. in combination with Alpert et al. have taught a computer system according to claim 1, as described above, and wherein the divert routine comprises a sequence of debug instructions, each debug instruction being associated with at least one debug attribute (column 1, lines 50-60, column 10, lines 38-65).

19. Referring to claim 7, Karp et al. in combination with Alpert et al. have taught a computer system according to claim 6, as described above, and wherein the last instruction in the divert routine includes a stall attribute which places the decode unit in a stall state (Alpert et al., column 11, lines 60-66, The process is suspended, or stalled at the next sequential instruction.).

20. Referring to claim 8, Karp et al. in combination with Alpert et al. have taught a computer system according to claim 6, as described above, and wherein the last instruction in the divert routine includes an atomic attribute which inhibits execution of any instruction other than the next instruction in the step-by-step sequence (Alpert et al., column 11, lines 60-66, This is precisely ho single-stepping works.).

21. Referring to claim 9, Karp et al. in combination with Alpert et al. have taught a computer system according to claim 6, as described above, and wherein the last instruction in the divert routine restores the interrupted instruction sequence (Alpert et al., Figure 2, element 250).

22. Referring to claim 11, Karp et al. in combination with Alpert et al. have taught a computer system according to claim 1, as described above. They have not specifically taught that the system includes a microinstruction generator which receives instructions from the decode unit and supplies microinstructions to the execution pipeline, said microinstructions including fields for holding respective guards to be resolved. However, it would have been obvious to implement the system of Karp et al. and Alpert et al. in microcode in order to increase the flexibility of the system. Implementing the system of Karp et al. and Alpert et al. in microcode would yield the claimed invention. Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to have the system of Karp et al. and Alpert et al., include a microinstruction generator which receives instructions from the decode unit and supplies microinstructions to the execution pipeline, said microinstructions including fields for holding respective guards to be resolved, for the desirable purpose of implementing the system in microcode, which increases the flexibility of the system.

23. Referring to claim 12, Karp et al. in combination with Alpert et al. have taught a computer system according to claim 1, as described above, and which includes a plurality of parallel pipelined execution units (Karp et al., figure 2, element 30), including at le1ast two data unit pipelines for executing data processing instructions (Karp et al., figure 2, element 30, Functional units for executing values in the register file.) and at least two address unit pipelines

for executing memory access instructions (Karp et al., figure 2, element 30, Functional units for executing memory operations.).

24. Claim 13 does not recite limitations above the claimed invention set forth in claim 1 and is therefore rejected for the same reasons set forth in the rejection of claim 1 above.

25. Referring to claim 14, Karp et al. in combination with Alpert et al. have taught a method according to claim 13, as described above, and wherein guard resolution is effected in a pipelined execution unit for executing said instructions (Karp et al., Column 5, line 23-column 6, line 3, When the guard resolves that the instruction is not committed, the instruction does not execute.).

26. Claim 15 does not recite limitations above the claimed invention set forth in claim 7 and is therefore rejected for the same reasons set forth in the rejection of claim 7 above.

27. Claim 16 does not recite limitations above the claimed invention set forth in claim 8 and is therefore rejected for the same reasons set forth in the rejection of claim 8 above.

28. Claim 18 does not recite limitations above the claimed invention set forth in claim 2 and is therefore rejected for the same reasons set forth in the rejection of claim 2 above.

29. Claim 20 does not recite limitations above the claimed invention set forth in claim 8 and is therefore rejected for the same reasons set forth in the rejection of claim 8 above.

30. Claim 21 does not recite limitations above the claimed invention set forth in claim 10 and is therefore rejected for the same reasons set forth in the rejection of claim 10 above.

31. Claim 23 does not recite limitations above the claimed invention set forth in claim 1 and is therefore rejected for the same reasons set forth in the rejection of claim 1 above.

32. Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Karp et al., US Patent 5,748,936, in view of Alpert et al., US Patent 5,621,886, and Page, Reconfigurable Processors, Oxford University Hardware Compilation Group Invited Keynote Address for Heathrow PLD Conference.

33. Referring to claim 2, Karp et al. in combination with Alpert et al. have taught a computer system according to claim 1, as described above. They have not specifically taught that the invention is implemented on a single chip. However, implementing the design on a single chip would yield a reduction in the number of parts and speed up communications between the parts, as taught by Page (Page, page 6, section 6, first paragraph). Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to have the invention of Karp et al. and Alpert et al. be implemented on a single chip, as taught by Page, for the desirable purpose of reducing the number of parts and speeding up communication between the parts (Page, page 6, section 6, first paragraph).

34. Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Karp et al., US Patent 5,748,936, in view of Alpert et al., US Patent 5,621,886, and Swoboda, US Patent 5,828,824.

35. Referring to claim 10, Karp et al. in combination with Alpert et al. have taught a computer system according to claim 1, as described above. They have not specifically taught that the invention is connected to a host computer which can take over operation of the emulation unit responsive to certain debug conditions. However, Swoboda have taught connecting a host computer to take over operation of an emulation unit in order to provide a powerful development tool (Swoboda, column 6, lines 18-39, column 7, line 25-45). It would have been obvious to one

of ordinary skill in the art at the time the invention was made to have the invention of Karp et al. and Alpert et al. be connected to a host computer which can take over operation of the emulation unit responsive to certain debug conditions for the desirable purpose of providing a powerful development tool (Swoboda, column 6, lines 18-39, column 7, line 25-45).

Conclusion

36. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tonia L Meonske whose telephone number is (703) 305-3993. The examiner can normally be reached on Monday-Friday, 9-6:30, with every other Friday off.

37. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie P Chan can be reached on (703) 305-9712. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

38. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

tlm

RICHARD L. ELLIS
PRIMARY EXAMINER